In order to advance prosecution of the present application, applicants have amended Claims 1 and 12 so as to positively recite the methods disclosed and illustrated in the specification of the present application. Specifically, applicants have amended the claims to positively recite that in step (a) of Claims 1 and 12 the pad stack includes at least a top patterned masking layer *that exposes portions of said pad stack.* Support for this amendment to Claims 1 and 12 is found at Page 8, lines 5-16 as well as in FIG 2.

Applicants have also amended step (c) of Claims 1 and 12 to positively recite that the first apertures or first trench isolation regions are formed using said patterned masking layer by first removing exposed portions of the pad stack to expose portions of the substrate abutting the patterned masking layer and then removing the exposed portion of said substrate. Support for this amendment to Claims 1 and 12 is found at Page 8, line 18-Page 9, line 7 as well as in FIGS 3 and 4.

Applicants have also amended step (e) of Claims 1 and 12 to positively recite that the second apertures or second trench isolation regions are formed using said patterned masking layer by first removing exposed portions of the pad stack to expose portions of the substrate abutting the patterned masking layer and then removing the exposed portion of said substrate. Support for this amendment to Claims 1 and 12 is found at Page 9, lines 9-23 as well as in FIGS 5 and 6.

Since the above amendments to Claims 1 and 12 do not introduce any new matter into the instant application, entry thereof is respectfully requested. Pursuant to 37 C.F.R. §1.121, applicants have attached a marked-up version of Claims 1 and 12 showing the changes made by the present amendment. The attached is captioned as "**MARKED-UP VERSION SHOWING CHANGES MADE**".

Claims 1-3, 5-14, and 16-20 stand rejected under 35 U.S.C. §103 as allegedly unpatentable over the combined disclosures of U.S. Patent No. 5,298,450 to Verret ("Verret") and U.S. Patent No. 5,950,093 to Wei ("Wei"). Claims 4 and 15 stand rejected under 35 U.S.C. §103 as allegedly unpatentable over the combined disclosures of Verret, Wei, and U.S. Patent No. 6,150,212 to Divakaruni, et al. ("Divakaruni, et al.").

Applicants respectfully submit that the combined disclosures of Verret and Wei, or Verret, Wei and Divakaruni, et al. do not render applicants' claimed methods obvious since none of the applied references teaches or suggests a method which includes, among other steps: *forming a plurality of apertures (or first trench isolation regions) having a first depth in an unblocked region of a semiconductor substrate using a patterned masking layer to define the plurality of first trench isolation regions by first removing exposed portions of a pad stack to expose portions of said substrate abutting said patterned masking layer and then removing said exposed portion of said substrate; and forming a plurality of second aperture (or trench isolation regions) having a second depth in regions of said semiconductor substrate that were previously blocked by a first block mask using said patterned masking layer to define said second trench isolation regions, while simultaneously increasing said first depth such that said first depth is deeper than said second depth, said second trench isolation regions are formed by first removing said exposed portions of said pad stack to expose portions of said substrate abutting said patterned masking layer and then removing said exposed portion of said substrate.* Thus, in the claimed methods, the initial patterned masking layer of the pad stack is used in defining both the first and second apertures.

Verret discloses a method which includes the steps of depositing a SiN layer 34 and a first photoresist layer on a surface of substrate 30 which includes SiO_2 layer 32 formed

thereon; patterning the first photoresist layer to provide patterned photoresist 36 which has openings that expose SiN layer 34; etching the exposed SiN layer and removing the first photoresist layer; forming second photoresist layer 42 having opening 44 on the now patterned SiN layer; etching a first trench 46 into the substrate through opening 42; removing the second photoresist layer; and etching to provide second trench 52 while deepening the first trench.

Thus, in Verret, a first masking layer 36 is required to pattern SiN layer 34, and neither the first masking layer nor the patterned SiN layer is used to define the first trench or aperture. Instead, a second patterned photoresist is used in defining the first trench. In the claimed methods, however, the first apertures (or first trench isolation regions) having a first depth are formed using the patterned masking layer of the initial pad stack by first removing exposed portions of a pad stack to expose portions of said substrate abutting said patterned masking layer and then removing said exposed portion of said substrate.

In forming the second trench, Verret employs the patterned SiN layer as a masking layer which defines the second trench. In the claimed method, the initial patterned masking layer of the pad stack is used in defining the second apertures or trenches. Applicants thus submit that in Verret extra critical masks and processing steps are needed to define the trenches having different depths.

Wei does not alleviate the above defects in Verret since the applied secondary reference also does not teach or suggest a method which includes steps of: *forming a plurality of apertures (or first trench isolation regions) having a first depth in an unblocked region of a semiconductor substrate using a patterned masking layer to define the plurality of first trench isolation regions by first removing exposed portions of a pad stack to expose portions of said*

substrate abutting said patterned masking layer and then removing said exposed portion of said substrate; and forming a plurality of second aperture (or trench isolation regions) having a second depth in regions of said semiconductor substrate that were previously blocked by a first block mask using said patterned masking layer to define said second trench isolation regions, while simultaneously increasing said first depth such that said first depth is deeper than said second depth, said second trench isolation regions are formed by first removing said exposed portions of said pad stack to expose portions of said substrate abutting said patterned masking layer and then removing said exposed portion of said substrate. Thus, in the claimed methods, the initial patterned masking layer of the pad stack layer is used in defining both the first and second apertures.

Wei provides a method for aligning a shallow trench isolation region which comprises the steps of forming deep alignment mark 202 in a surface of substrate 200; forming pad oxide layer 204 on the surface of the substrate including the walls of the deep alignment mark 202, forming SiN layer 206 atop pad oxide layer 204; forming a patterned photoresist on SiN layer 206 and removing SiN, pad oxide and substrate that are not protected by the photoresist so as to form a plurality of trenches 208a, while removing exposed portion of alignment mark 202.

Applicants respectfully submit that in Wei the same masking layer is not used in defining the alignment mark or the trenches; therefore the claims of the present application are not obvious from Wei. As such, applicants submit that the combination of Verret and Wei does not render applicants' claimed methods obvious.

The other applied reference cited in the present Office Action, i.e., Divakaruni, et al., is further removed from the claimed method than either Verret or Wei as evident by the fact

that the Examiner has relied on Divakaruni, et al. for disclosing the types of patterned masking layers defined in dependent Claims 4 and 15. Applicants find no disclosure in Divakaruni, et al. which teaches or suggests using the patterned masking layer to define a first trench, and thereafter a second trench, wherein the first trench is deeper than the second trench. As such, the combination of Verret, Wei and Divakaruni, et al. does not render applicants' claimed method obvious.

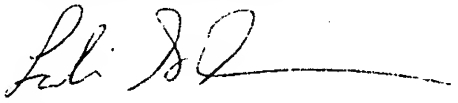
The §103 rejections also fail because there is no motivation in the applied references which suggests modifying the methods disclosed therein to include applicants' claimed method which includes the processing steps of *forming a plurality of apertures (or first trench isolation regions) having a first depth in an unblocked region of a semiconductor substrate using a patterned masking layer to define the plurality of first trench isolation regions by first removing exposed portions of a pad stack to expose portions of said substrate abutting said patterned masking layer and then removing said exposed portion of said substrate; and forming a plurality of second aperture (or trench isolation regions) having a second depth in regions of said semiconductor substrate that were previously blocked by a first block mask using said patterned masking layer to define said second trench isolation regions, while simultaneously increasing said first depth such that said first depth is deeper than said second depth, said second trench isolation regions are formed by first removing said exposed portions of said pad stack to expose portions of said substrate abutting said patterned masking layer and then removing said exposed portion of said substrate.* This rejection is thus improper since the prior art does not suggest this drastic modification. The law requires that a prior art reference provide some teaching, suggestion, or motivation to make the modification obvious.

Here, there is no motivation provided in the disclosures of the applied prior art references, or otherwise of record, which would lead one skilled in the art to modify the methods of the applied references to include applicants' claimed sequence of processing steps recited in amended Claims 1 and 12 that lead to the formation of apertures or trenches of different depths. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Fritch, 972 F.2d, 1260,1266, 23 USPQ 1780,1783-84 (Fed. Cir. 1992).

Based on the above amendments and remarks, the §103 rejections have been obviated; therefore reconsideration and withdrawal of the instant rejections are respectfully requested.

Wherefore reconsideration and allowance of the claims of the present application are respectfully requested.

Respectfully submitted,



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ATTACHMENT: MARKED-UP VERSION SHOWING CHANGES MADE IN THE CLAIMS:

Please amend Claims 1 and 12 to read as follows:

1. (Amended) A method for forming multi-depth apertures in a substrate comprising the steps of:

(a) providing a pad stack atop a surface of a substrate having regions for forming apertures therein, said pad stack including at least a top patterned masking layer that exposes portions of said pad stack;

(b) blocking at least one of said regions of said substrate with a first block mask, while leaving at least one other region of said substrate unblocked;

(c) forming a plurality of first apertures having a first depth in said unblocked region of said substrate using said patterned masking layer to define said plurality of first apertures by first removing said exposed portions of said pad stack to expose portions of said substrate abutting said patterned masking layer and then removing said exposed portion of said substrate;

(d) removing said first block mask; and

(e) forming a plurality of second apertures having a second depth in regions of said substrate that were previously blocked by said first block mask using said patterned masking layer to define said second apertures, while simultaneously increasing said first depth such that said first depth is deeper than said second depth, said second apertures are formed by first removing said exposed portions of said pad stack to expose portions of said substrate abutting said patterned masking layer and then removing said exposed portion of said substrate.

12. (Amended) A method of forming multi-depth isolation regions in a semiconductor substrate comprising the steps of:

(a) providing a pad stack atop a surface of a semiconductor substrate having regions for forming trench isolation regions therein, said pad stack including at least a top patterned masking layer that exposes portions of said pad stack;

(b) blocking at least one of said regions of said semiconductor substrate with a first block mask, while leaving at least one other region of said semiconductor substrate unblocked;

(c) forming a plurality of first trench isolation regions having a first depth in said unblocked region of said semiconductor substrate using said patterned masking layer to define said plurality of first trench isolation regions by first removing said exposed portions of said pad stack to expose portions of said substrate abutting said patterned masking layer and then removing said exposed portion of said substrate;

(d) removing said first block mask; and

(e) forming a plurality of second trench isolation regions having a second depth in regions of said semiconductor substrate that were previously blocked by said first block mask using said patterned masking layer to define said second trench isolation regions, while simultaneously increasing said first depth such that said first depth is deeper than said second depth, said second trench isolation regions are formed by first removing said exposed portions of said pad stack to expose portions of said substrate abutting said patterned masking layer and then removing said exposed portion of said substrate.